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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,525	09/29/2003	John Bruno	00100.03.0034	6091

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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

MAIL DATE	DELIVERY MODE
03/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/675,525	BRUNO ET AL.	
	Eric Chang	Art Unit 2116	

Document Code - AP.PRE.DEC

Notice of Panel Decision from Pre-Appeal Brief Review

This is in response to the Pre-Appeal Brief Request for Review filed Jan. 16, 2008.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
☐ The request does not include reasons why a review is appropriate.
☐ A proposed amendment is included with the Pre-Appeal Brief request.
☐ Other:

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☒ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☒ The panel has determined the status of the claim(s) is as follows:
Claim(s) allowed: _____.
Claim(s) objected to: 47.
Claim(s) rejected: 12, 13, 15-19, 34 and 44-46.*
Claim(s) withdrawn from consideration: _____.
* See attachment.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☐ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) Eric Chang.

(2) Rehana Perveen.

(3) Eddie C. Lee.

(4) _____.

As to claim 12, Williams discloses a clock control system for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, comprising: a thermal sensor operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die [302]; a thermal sensor control circuit, operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal [701] and to provide an interrupt control signal in response to the temperature data [702]; a clock generator circuit operative to produce the clock signal [101]; and a dynamic overclock frequency control data generator [102], operatively coupled to the thermal sensor control circuit and the clock generator circuit [FIGS. 1 and 2B], and operative to provide dynamic overclock frequency control data to the clock generator circuit in response to the received temperature data [701] to cause the clock generator circuit to increase the operating frequency of the clock signal above the nominal operating frequency [709], when the detected junction temperature is less than the maximum rated junction temperature [702]. Williams teaches a clock control system that increases the operating frequency of the clock if the detected temperature does not indicate an overheat condition, that is, it is less than a maximum rated junction temperature.

As to claim 17, Williams discloses a method for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, the method comprising: detecting a junction temperature corresponding to at least a portion of a circuit on a die [701]; and increasing the operating frequency of the clock signal above the nominal operating frequency [709], when the detected junction temperature is below the maximum rated junction temperature [702].

As to claim 34, Williams discloses a clock control system for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, comprising: a thermal sensor operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die [302]; a thermal sensor control circuit, operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal [701] and to provide an interrupt control signal in response to the temperature data [702]; a clock generator circuit operative to produce the clock signal [101]; and a dynamic overclock frequency control data generator [102], operatively coupled to the thermal sensor control circuit and the clock generator circuit [FIGS. 1 and 2B], and operative to provide dynamic overclock frequency control data to the clock generator circuit in response to the received temperature data [701] to cause the clock generator circuit to increase the operating frequency of the clock signal above the nominal operating frequency [709], when the detected junction temperature is less than the maximum rated junction temperature [702]. In addition, Bailey teaches a memory [136] comprising data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies [col. 5, lines 28-46, and col. 5, line 62 thru col. 6, line 17].

As to claim 45, Williams discloses a clock control system comprising: detecting a junction temperature corresponding to at least a portion of a circuit on a die [701]; and

increasing the operating frequency of the clock signal above the nominal operating frequency [709], when the detected junction temperature is below the maximum rated junction temperature [702]. In addition, Bailey teaches a memory [136] comprising data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies [col. 5, lines 28-46, and col. 5, line 62 thru col. 6, line 17].